3E2075

Roll No. : _____ Total Printed Pages : 3

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B.Tech. (Sem. III) (Main/Back) Examination, January - 2012
Digital Electronics
(Common for Comp. Engg. & IT)

Time : 3 Hours] [Total Marks : 80
[Min. Passing Marks : 24

Instructions to Candidates :

*Attempt any **five questions** selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. Nil 2. _____

UNIT-I

1 (a) What is meant by the base of number system ? Give example to illustrate the role of the base in positional number system. **6**

(b) Convert the following numbers from the given base to the other base indicate –

(i) Binary $(11011101)_2 \rightarrow (?)_{10}, (?)_8$

(ii) Octal $(632.25)_8 \rightarrow (?)_{10}, (?)_{Hex}$

(iii) Hex $(2AC5.2B)_{16} \rightarrow (?)_{10}, (?)_{Octal}$ **10**

OR

1 (a) Find by inspection the complement of each of the following expression and then simplify it.

(i) $\bar{x}\left(\bar{y}+\bar{z}\right)\left(x+y+\bar{z}\right)$

(ii) $\left(x+\bar{y}+\bar{z}\right)\left(y+\overline{\bar{x}z}\right)\left(z+\overline{\bar{x}y}\right)$

(iii) $\bar{w}+\left(x+y+\overline{\bar{y}z}\right)\left(x+\bar{y}z\right)$

(b) Define Universal Logic Gates. Redraw the circuit Figure 1 using Universal Logic Gates.

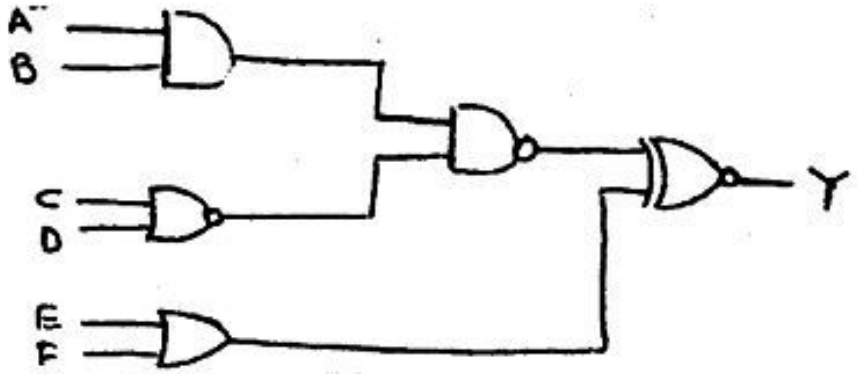

Fig. 1

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UNIT-II

2 (a) Define the (i) noise immunity and (ii) Fanout. Draw the internal structure of TTL tristate gate and explain its operation.

8

(b) Explain the parameters used to characterize logic families. Calculate the noise margin of ECL gate.

8

OR

2 (a) Draw the circuit for CMOS inventer. What are the different schemes for CMOS to TTL interface. Explain one of them.

8

(b) Explain how a MOS can be used as a switch in a digital circuit ? How does a TTL gate differ from MOS gate ?

8

UNIT-III

3 (a) Obtain minimum SOP expression for following Boolean expression using Karnaugh Map.

$F = \sum m(0,1,2,5,7,9,13,15) + d(8,11)$

Realise the minimised function using logic gates.

8

(b) Implement the following boolean function with NOR-NOR gate logic.

$Y = AC + BC + D$

8

OR

3 (a) Explain briefly the systematic procedure for using don't care condition. Define multilevel logic circuit with diagram.

8

(b) What are the advantages of tabulation method ? A staircase light is controlled by two switches, one at the top of the stairs and another at the bottom of the staircase.

(i) Make a truth table for this system.

(ii) Write logic equation

(iii) Realize the circuit using AND – OR gates.

8

UNIT-IV

4 (a) How you use a decoder as a ROM ? Design a 5 to 32 decoder using one 2 to 4 and Four 3 to 8 decoder ICs.

8

(b) Explain the Code Converter. Design a Code Converter that converts a BCD code from the 5421 code.

8

OR

4 (a) Explain the operation of binary serial and parallel adder with schematic diagram.

8

(b) Explain diode switching matrix in briefly. Design a binary multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders.

8

UNIT-V

5 (a) Explain the procedure to convert one Flip Flop to another Flip Flop. Explain how the J. K. Flip Flop can be converted into a T Flip Flop.

8

(b) Explain the operation of a Master Slave Flip Flop and show how the race around condition is eliminated.

8

OR

5 (a) Explain the working of Serial in Parallel Out Shift register with logic diagram and waveform.

8

(b) What is Modulus Counter ? Draw the state diagram of a modulo-4 UP/DOWN counter. Design its circuit using J. K. Flip Flops.

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