3E1137

Roll No.

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B. Tech. III - Sem. (Main) Exam., Dec. - 2018

ESC Computer Science & Engineering

3CS3 – 04 Digital Electronics

CS, IT

Time: 3 Hours **Maximum Marks: 120**

Instructions to Candidates:

Attempt all ten questions from Part A, selecting five questions from Part B and four questions from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 Convert $(D2.9)_{16} = (\ )_8$

Q.2 Find the sum $(y)_6 = (5.2)_6 + (4.5)_6$

Q.3 Convert $Y = A + B\bar{C} + A\bar{B} + A\bar{B}C$ into canonical form.

Q.4 Find the minimum number of nand gate required to realize $Y = A\bar{B}C$.

Q.5 Find the value of x

$(23)_x + (12)_x = (101)_x$

Q.6 Explain the reflected code.

Q.7 Implement a latch using 2:1 mux.

Q.8 State the difference between combinational and sequential circuit.

Q.9 Write the RS flip flop excitation table.

Q.10 How many JK flip flop are required to implement modulus 50 counters?

PART – B

(Analytical/Problem solving questions) **[5×8=40]**

Attempt any five questions

Q.1 The two numbers represented in signed 2's complement form are P = 11101101 and Q = 11100110. Find the value obtained in signed 2's complement form for P – Q.

Q.2 Simplify the following function and implement it using NOR gate –

$$F = A\bar{B} + ABD + AB\bar{D} + \bar{A}\bar{C}\bar{D} + \bar{A}B\bar{C}$$

Q.3 Implement the following logic using only one 8:1 MUX –

$$F(A, B, C, D) = \sum m(1, 3, 4, 11, 12, 13, 14, 15)$$

Q.4 Explain prime, essential and redundant implicant using suitable example.

Q.5 State the merits and demerits of various logic families.

Q.6 Convert JK flip flop into RS flip flop. Explain its process also.

Q.7 A stair case light is controlled by two switches one at top of stairs and another at bottom of stairs. Realize the circuit using minimum number of NOR gate when lamp (L) glows.

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[4×15=60]**

Attempt any four questions

Q.1 Using JK flip flop design a synchronous counter that counts in sequence –

000, 001, 110, 011, 010, 111, 101, 100, 000

Q.2 Simplify the following function using tabulation method and verify the result using K-map

$F = \Sigma (0, 6, 9, 10, 13) + d (1, 3, 8)$

Q.3 Draw a neat circuit diagram of TTL (Transistor Transistor Logic) NAND gate with totem pole output and explain.

Q.4 Determine the next state for each of six unused states in BCD ripple counter. Is the counter self starting? Design a divide by 8 counter also.

Q.5 Write short note on only two –

(a) Universal gate

(b) ASCII code

(c) Weighted code

(d) High threshold logic
