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B.Tech. VI Sem. (Main/Back) Examination, June - 2022
Information Technology
6IT4-04 Computer Architecture and Organization

Time : 3 Hours **Maximum Marks : 120**

Min. Passing Marks : 42

Instructions to Candidates:

*Attempt **all ten** questions from **Part A**, **five** questions out of **Seven** from **Part B** and **Four** questions out of **Five** from **Part C**.*

Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No.205)

Part - A
(Answer should be given up to 25 words only)

All questions are **compulsory** **(10×2=20)**

1. What do you mean by computer performance? **(2)**
2. If the memory is represented in 12 bits × 16 bits then how many words can be accommodated in the memory? **(2)**
3. Describe subroutine? **(2)**
4. What do you mean by Hit Ratio in cache memory? **(2)**
5. Write a quick note on Interrupt intiated input - output? **(2)**
6. Discuss on concept of parallel processing? **(2)**
7. Explain the concept of microprogrammed control unit? **(2)**
8. Convert +1001.11 in 8 bit fraction and 6 bit exponent as per floating point representation. **(2)**
9. Describe the three fields (Mode, Opcode and Address field) of 16 bit instruction format. **(2)**
10. Perform selective component over **(2)**
    A = 1011 0110 and B = 0110 1110.

Part - B
(Analytical/Problem solving questions)

Attempt any **five** questions **(5×8=40)**

1. Draw the flow diagram for the hardware that implements the following statements - **(8)**
   $X + yz : AR \leftarrow AR + BR$
   Where AR and BR are two n - bit registers and x y and z are control variable. Include the logic gates for the control function. (Remember that the symbol '+' designates an OR operation in a control or Boolean function but that it represents and arithmetic plus in a micro operation.

2. What is priority interrupt? Explain Daisy chaining Priority Interrupt's polling logic using its block diagram and logical diagram both. (8)

3. A non - pipeline system takes 100 ns to process a task. The same task can be processed in a six - segment pipeline with a clock cycle of 20 ns. Determine the speed - up ratio of pipeline for 200 tasks. What is maximum speed - up that can be achieved? (8)

4. Explain the functional units of an architecture of computer with diagram? (8)

5. Explain the types of instructions? (8)

6. Differentiate between Hardwired and Micro - programmed control unit? (8)

7. Explain significance of data register, address register, instruction register, temporary register, program counter and accumulator in common bus system. (8)

Part - C

(Descriptive/Analytical/Problem Solving/Design questions)

Attempt any **Four** questions (4×15=60)

1. Perform Multiplication of -13 and +9 using Booth Algorithm. With the help of diagram. Explain line coding schemes. (15)

2. A digital computer has a common bus system for 8 registers and 16 bits each. The bus is constructed with multiplexers. (15)
   a. How many selection inputs are there in each multiplexer?
   b. How many multiplexers are there in the bus?
   c. What size of multiplexers is needed?
   d. Draw the diagram of the mentioned problem definition.

3. Explain the need of cache memory. What is Hit Ratio? Elaborate over the three types of mapping under cache memory with neat diagram. (15)

4. Why pipeline is useful in processing? Explain instruction pipeline including the processing steps used in pipeline. Explain speedup, efficiency and through put in pipelining. Prove that ratio of non pipeline based architecture and pipeline based architecture depends upon the no. of segments (k). (15)

5. a. How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes? (15)
   b. How many lines of address bus must be used to access 2048 bytes of memory? How many of These lines will be common to all chips?
   c. How many lines must be decoded for chip select?
   d. Specify the size of the decoders?