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7E7086

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B.Tech. VII -Semester (Main&Back) Examination, Nov. - 2019
Electronics And Comm. Engg.
7EC6.3A VHDL

Time : 3 Hours

Maximum Marks : 80
Min. Passing Marks : 26

Instructions to Candidates:

Attempt any five questions, selecting one question from each unit. All Questions carry equal marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly). Units of quantities used/calculated must be stated clearly.

UNIT - I

1. a) What is the difference between CPLD and FPGA? Explain both of them according to their applications. **(10)**

   b) What is routing? Explain briefly. **(6)**

(OR)

1. a) Write about the design flow for ASIC. **(8)**

   b) State the difference between synthesis and simulation and explain the logic synthesis in detail. **(8)**

UNIT - II

2. Define the following in VHDL :

   i) Entity

   ii) Architecture

   iii) Package

   iv) Configuration **(16)**

(OR)

2. a) What is VHDL? Explain advantage and limitations of VHDL. **(8)**

   b) Write short note on

   i. Behavioral Modelling

   ii. Structural modelling. **(8)**

UNIT - III

3. a) Write a VHDL code for 1:16 line decoder. (8)

b) Consider the function

$$Y = \overline{A}BC + \overline{AB}C + AB\overline{C}$$

Impliment the above function using 2:1 multiplexer and also write the VHDL code for it. (8)

(OR)

3. Write a VHDL code for following :

a. JK flip flop

b. D flip flop using JK flip flop.

c. T flip flop

d. 3 - Input XOR gate. (16)

UNIT - IV

4. a) What is finite state machine : (4)

b) Design a moore type FSM to detect 101 non overllaping sequence. Also design the synchronous sequential circuit using D - flip flop. (12)

(OR)

4. a) Write a VHDL code for serial adder. (8)

b) State the difference between mealey and moore type FSM. (8)

UNIT - V

5. a) Draw a schematic diagram of data path circuit for multiplier operation. (8)

b) What problems occur during clock synchronization? Also explain the techniques to avoid them. (8)

(OR)

5. a) What is memory organization? Explain 6 T SRAM in detail. (8)

b) How external devices are interfaced with CPU? Explain in detail. (8)