7E7086

Roll No. _____

Total No of Pages: 3

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B. Tech. VII - Sem. (Back) Exam., Feb.-March - 2021
Electronics & Communication Engineering
7EC6.3A VHDL

Time: 2 Hours

Maximum Marks: 48
Min. Passing Marks: 15

Instructions to Candidates:

Attempt three questions, selecting one question each from any three unit. All Questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No.205)

1. NIL 2. NIL

UNIT- I

Q.1 Explain the following terms in VHDL-

(a) Functional Simulation [4]

(b) Timing Simulation [4]

(c) Design Flow [4]

(d) Design Methodology [4]

OR

Q.1 Write VHDL code for -

(a) Full Adder [4]

(b) 2 × 1 MUX [4]

(c) 3 – input NOR gate [4]

(d) SR – Latch – [4]

UNIT- II

Q.2 How the following is defined/written in VHDL :-

(a) Event driven Simulation [4]

(b) Data Types [4]

(c) Signals Verses Variables [4]

(d) Packages [4]

Explain with an example.

OR

Q.2 (a) Write VHDL code for a 4 – bit down counter using sequential statements. [8]

(b) Define elaboration, signal driver using an example. [8]

UNIT- III

Q.3 (a) Write VHDL code for a 4 – bit shift register. [8]

(b) Write VHDL code for a code converter (Consider any one example). [8]

OR

Q.3 (a) Write VHDL code for JK flip-flop in two styles. [8]

(b) Write a VHDL code for 7 – segment to BCD code converter using select signal assignment. [8]

UNIT- IV

Q.4 (a) Write a VHDL code for a Moore m/c and explain the general procedure for such a m/c. [8]

(b) Identify shift register as Moore or Mealy m/c and write its VHDL code accordingly. [8]

OR

Q.4 Write a VHDL code for a Vending Machine that delivers tea at a cost of ₹ 5 and accepts coins of ₹ 1, ₹ 2 and ₹ 5. [16]

UNIT- V

Q.5 (a) How memory organization is defined in VHDL? Write a VHDL code to organize 10k (SRAM) memory. [8]

(b) Explain the clock synchronization in VHDL. [8]

OR

Q.5 (a) Design a 4-bit divider and draw its flow diagram. Then write the VHDL code for it. [10]

(b) Explain shifting & sorting operation in VHDL. [6]