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7E7084

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B.Tech. VII- Semester (Main&Back) Examination, November - 2019
Electronics and Comm. Engg.
7EC5A VLSI Design

Time : 3 Hours **Maximum Marks : 80**
Min. Passing Marks : 26

Instructions to Candidates:

Attempt any five questions, selecting one question from each unit. All Questions carry equal marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly) Units of quantities used/calculated must be stated clearly.

UNIT - I

1. a) Develop the relation between I_{ds} and V_{ds} for MOSFET and modify it under channel length modulation. **(8)**

   b) Draw variation of gate oxide capacitance with V_{ds}. Assume the gate voltage $V_{gs} > v_{th}$. **(6)**

   c) State the condition of ohmic operation. **(2)**

OR

1. a) Find the expression of threshold voltage V_{tho} and discuss how it modified under body bias. **(8)**

   b) Discuss any two phenomena in MOSFET from.

   i) Hot electron effect

   ii) Subthreshold conduction

   iii) Narrow channel effect. **(4+4=8)**

UNIT - II

2. a) Draw NMOS inverter with active load and draw its Transfer characteristic. Also find the expression 7 V_{IL}, V_{IH}, V_{OL} and V_{OH} for it. **(10)**

   b) Draw $y = A + \bar{B}C$ using CMOS. **(6)**

OR

2. a) Draw and explain the working of Transmission gate (TG). Use it for 2×1 CMOS multiplexer. **(8)**

b) What is transistor sizing? Design a y = ABC CMOS logic such that its equivalent (D/L) of pull up section is 90 and pull down section is 30. (8)

Unit - III

3. a) Draw following CMOS Ckt
   i. y = A+BC+D
   ii. $y = \overline{A} + \overline{BC}$ (4+4=8)

   b) Draw the layout of y = AB+CDE CMOS ckt use Eular path in it. (8)

OR

3. a) What is Latch up Problem? How it can be avoided in CMOS ckts? (8)

   b) State any four DRC rules regarding:
   i. Contact size
   ii. Metal to Metal line separation.
   iii. Poly width and
   iv. Separation between pdiff and Ndiff. (4×2=8)

Unit - IV

4. Draw and explain any two logic Ckt from.
   i. NORA logic.
   ii. DRAM
   iii. DOMINO logic
   iv. NP logic. (2×8=16)

Unit - V

5. Write short note on any two :
   i. VHDL code
   ii. FPGA
   iii. Custom design
   iv. ASIC design (2×8=16)