7E1727

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B. Tech. VII - Sem. (Main) Exam., Feb.- March - 2021
PEC Electronics & Communication Engineering
7EC5 - 11 VLSI Design

Time: 2 Hours **[To be converted as per scheme]**

Max. Marks: 82

Min. Marks: 29

Instructions to Candidates:

Attempt all ten questions from Part A, four questions out of seven questions from Part B and two questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 Write down the equations for Ids of an n-channel enhancement MOSFET operating in Non-saturated region and saturated region.

Q.2 Draw the circuit diagram for CMOS two-input NAND gates.

Q.3 Draw the basic circuit of NMOS and CMOS inverter.

Q.4 What are the advantages and disadvantages of dynamic logic?

Q.5 What parameters to be consider while identifying the FPGA?

Q.6 What is NORA CMOS?

Q.7 What is meant by channel length modulation in NMOS transistors?

Q.8 Differentiate between SRAM and DRAM?

Q.9 Draw a 1 – Transistor dynamic RAM cell.

Q.10 Mention different clocking mechanisms.

PART – B

(Analytical/Problem solving questions) **[4×8=32]**

Attempt any four questions

Q.1 What is threshold voltage of a MOS device and explain its significance.

Q.2 Prove that the pull-up to pull-down for NMOS inverter is 4:1 when it is driven by another inverter.

Q.3 What is "Euler path"? What is use of it? Explain with a suitable example.

Q.4 Draw the CMOS logic circuit for the Boolean expression Z=[A(B+C) +DE] and explain.

Q.5 What is a stick diagram and explain about different symbols used for components in stick diagram?

$\bar{A} + \{\bar{B} \cdot \bar{C} \cdot (\bar{D} + \bar{E})\}$

$\bar{A} \cdot \{\bar{B} + \bar{C} + \bar{D}\bar{E}\}$

Q.6 Derive the propagation delay for NMOS inverter?

Q.7 Explain the Domino logic with neat diagram.

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[2×15=30]**

Attempt any two questions

Q.1 Explain the dynamic behavior of MOSFET transistor with neat diagram.

Q.2 Write the layout design rules and draw diagram for four input NAND and NOR gate.

Q.3 Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions.

Q.4 Explain about building block architecture of FPGA.

Q.5 What do you mean by VHDL? Write a VIDL code for-

(a) Full Adder

(b) D Flip-flop